The Co-operative University of Kenya

END OF SEMESTER EXAMINATIONS DECEMBER-2019

EXAMINATION FOR THE DEGREE OF BACHELOR OF SCIENCE IN COMPUTER SCIENCE

(YR IV SEM II)

UNIT CODE: BCSC 1138

UNIT TITLE: ELECTRONICS I

DATE: 9th DECEMBER 2019 **TIME: 9:00 AM – 11:00 AM**

INSTRUCTIONS:

Answer question **ONE (compulsory)** and any other **TWO** questions

QUESTION ONE

(a) Giving examples differentiate between passive and active electronic circuit components (4 marks)

(b) Explain the following electronic circuit elements (6 marks)

i. Capacitor
ii. Inductor
iii. Diode

(c) Using a neat diagram explain the I-V characteristics of a PN Junction diode (8 marks)

(d) Explain how the potential barrier is developed on PN junction (4 marks)

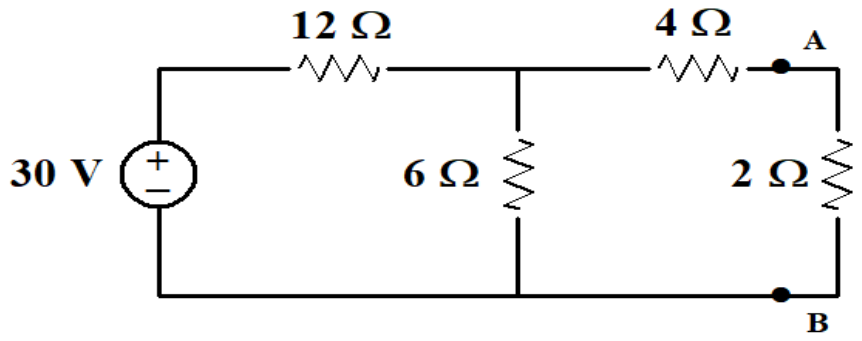
(e) Using a neat diagram explain the **THREE** operation regions of a BJT. State the application of BJT in each region (7 marks)

QUESTION TWO

(a) Explain how the depletion layer is formed on the PN junction (2 marks)

(b) Differentiate between intrinsic and extrinsic semiconductors (4 marks)

(c) Using Thevenin`s Theorem calculate the voltage drop across the 2Ω resistor in the circuit shown below (8 marks)



(d) With the aid of diagrams, describe any two bipolar transistor biasing methods (6 marks)

QUESTION THREE

(a) State the structural and functional difference between NPN and PNP transistors (6 marks)

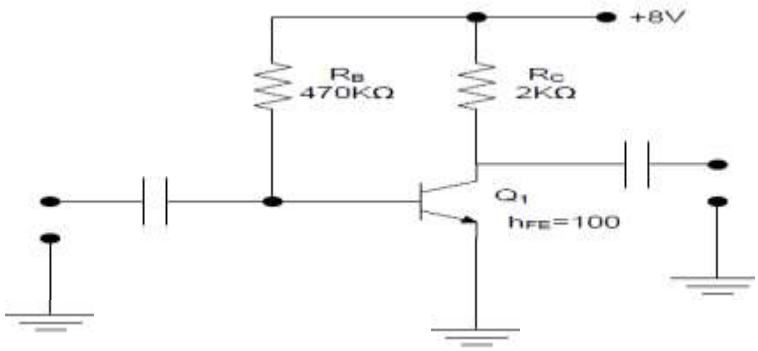
(b) In an NPN transistor $10^8\ holes/\mu s$ move from the base to the emitter region while $10^{10}\ electrons/\mu s$ move from the emitter to the base region. An ammeter reads the base current as $I_B = 16\mu A$. Determine the Emitter Current I_E and the collector current I_C. (4 marks)

(c) For the diagram of figure 3 below, determine:

a. Configuration of the transistor amplifier (2 marks)

b. Q-point (Values of I_C and V_{CE}) (3 marks)

c. Draw the DC load line (Label the value of the quiescent base current curve, I_B, and mark the Q-point.) (3 marks)



(d) Explain how the drain current is controlled in n-channel JFETs? (2 marks)

QUESTION FOUR

(a) Using a well labeled diagram, describe the working of an N-channel JFET. (12 marks)

(b) Using a neat diagram explain the voltage divider bias of a BJT. Show the expression for transistor collector voltage and collector emitter voltage (8marks)

QUESTION FIVE

(a) Explain the source of charge carriers in intrinsic semiconductors (2 marks)

(b) Explain the difference between JFET and MOSFET (4 marks)

(c) Draw the symbols for N-channel MOSFET and P-Channel MOSFET (4 marks)

(d) Explain three reasons why a JFET is preferred over a BJT (6 marks)

(e) Describe the characteristics of the JFET when operated in the ohmic region. (4 marks)