The Co-operative University of Kenya

END OF SEMESTER EXAMINATIONS APRIL-2019

EXAMINATION FOR THE DEGREE OF BACHELOR OF SCIENCE IN INFORMATION TECHNOLOGY (YR I SEM II)

UNIT CODE: BCIT 1201

UNIT TITLE: COMPUTER DESIGN & ORGANIZATION

DATE: 25TH APRIL, 2019 **TIME: 2:00 PM – 4:00 PM**

INSTRUCTIONS:
Answer question **ONE (compulsory)** and any other **TWO** questions **Question one**

QUESTION ONE

(a) Define the concept ofComputer system as used in computer design (2 marks)
(b) With examples distinguish between Computer Architecture and Computer organization (4 marks)
(c) State the three main principles of computer (3 marks)
(d) Draw a block diagram of a computer system with five key components (5 Marks)
(e) With clear distinction, describe the five chronological generations of computer (7marks)
(f) Using a diagram, explain the Von Neumann Architecture for computers (5 marks)
(g) Perform a decimal addition in BCD Code (4 marks)
   i. 25 + 13
   ii. 679.6 + 536.8

QUESTION TWO

(a) What is Von Neumann bottleneck? (3 marks)
(b) State ANY TWO essential features of a Von Neumann machine (4 marks)
(c) Convert the 147_{10} to the binary equivalent (2 marks)
(d) Convert the binary fraction 0.11101 to decimal (2 marks)
(e) With an aid of a diagram explain the memory hierarchy concept. (5 marks)
(f) Explain the following terminology used in reference to message passing between processes communicating/connected through a network (4 marks)
   - Bandwidth
   - Message latency

QUESTION THREE

(a) Explain what is a computer architecture (4 marks)
(b) How does caching improve the performance of a computer system? (5 marks)
(c) Explain any TWO benefits of multithreading (4 marks)
(d) Briefly, explain the concept of Virtual Memory (3 marks)
(e) Add the following signed integers -93 and 44 using the following steps:
   i)Convert both integers to 8-bit 2's complement form. (2 marks)
   ii) Convert the 2's complement representation to decimal answer. (2 marks)

QUESTION FOUR

(a) Convert the binary number 10110010 to hexadecimal. (2 marks)
(b) Perform the following hexadecimal additions: A5A + 2F5 (2 marks)
(c) Describe the DMA operation in regard to data transfer in an i/o module. (6 marks)
(d) Explain software polling and bus arbitration as methods of servicing interrupts. (6 marks)
(e) Explain the error detection and correction in memory using parity bits technique. (4 marks)